REMARKS

The Examiner's Action mailed on December 1, 2003 has been received and its contents carefully considered. In this Amendment, the applicant has canceled claims 5 and 7-9, 11, 13-16 and 22-25, and amended claims 3, 6, and 10, 17, 19 and 21. Reexamination and reconsideration of the amended application respectfully is requested. For at least the following reasons, it is submitted that this application is in condition for allowance.

The Examiner has rejected all the pending claims 3-25 based on the teachings by *Sekine et al.* (WO99/09595), *Egawa* (JP 8-236692), *Fukasawa et al.* (US 6,455,920) and *Ichikawa* (JP 2-31437). Claims 13-16 and 22-25 have been canceled without prejudice or disclaimer. Claim 3 has been amended to include the limitations of claims 5, 7, 8 and 9, and claim 10 has been amended to include the limitations of claim 11, both to clarify the differences of the present invention from the prior cited art. The incorporated dependent claims and claims 5, 7, 8, 9 and 11 accordingly are canceled. Claim 17 has been amended to further clarify the invention.

First taking up a rejection of claims 3-9 under 37 USC 103(a) as being unpatentable over *Sekine et al.* (WO99/09595) in view of *Fukasawa et al.* (US 6,455,920) and *Ichikawa* (JP 2-31437), it is submitted that amended claim 3 clearly is patentable over this cited prior art, taken separately or in combination. Referring to

the reference numerals in the drawings (Figs. 3(a) to 3(f)) and specification for convenience of explanation only, amended claim 3 is directed to a method of manufacturing a semiconductor device, which includes the following steps:

forming projection electrodes T on the surface 1 of the semiconductor substrate (wafer W),

after the step of forming projection electrodes, forming a surface resin layer 3 on the substrate surface 1,

a surface grinding step of exposing the projection electrodes T from the surface resin layer 3 by polishing or grinding the surface resin layer 3,

after the surface grinding step, forming a back side resin layer 4 on a back side 2 of the semiconductor substrate W, and

thinning the semiconductor substrate W by removing the back side resin layer 4, through polishing or grinding, from the semiconductor substrate provided with the surface resin layer 3 and the back side resin layer 4, and by further polishing or grinding the back side 2 of the semiconductor substrate W from which the back side resin layer 4 has been removed, in which the surface resin layer 3 and the back side resin layer 4 are so formed as to have substantially the same thicknesses.

The Examiner relies upon *Fukasawa et al.* for a disclosure of formation of resin layers on the front and back surfaces of a semiconductor substrate. *Ichikawa* discloses formation of a resin layer on the back surface of a semiconductor substrate followed by grinding of a resin layer and then grinding the back surface of the semiconductor substrate. *Sekine et al.* disclose formation of bumps 46 on the front surface of a bare chip device 47 followed by sealing with epoxy resin 48 and then grinding or polishing the front surface until the bumps 46 are exposed.

However, none of the cited references teach or suggest that a surface grinding step is performed before a back side grinding step as recited in original claim 8 and now in amended claim 3. As to claim 8, Examiner states in the Action, that "[t]he transposition of process steps where the processes are substantially identical or equivalent in terms of function, manner and result was held to be not patentably distinguish the processes (*Ex parte Rubin* 128 USPQ 159)." This is not the case in the present invention, however. That is, as discussed in the following, in the present invention as defined in amended claim 3, the processes are <u>not</u> substantially identical or equivalent in terms of function, manner and result.

One advantage of this claimed feature, as is described at lines 15-18 on page 13 in the present specification, is that the claimed order of grinding or polishing the surface and back side resin layers facilitates obtaining a uniform thickness of the front side protective resin layer by avoiding warping of the wafer. That is, the thickness of the protective resin layer 3 on the front surface of a wafer W can be made uniform in any portion of the semiconductor substrate (wafer W in the drawings) if the surface grinding step is performed first. To the contrary, if the back side grinding step is performed first, then the wafer W may be warped at the time of the front side grinding step due to the difference in the thickness between the front side resin layer and back side resin layer. This, in turn, results in non-uniform thickness of the front side protective resin layer 3. Thus, contrary to the assertion by the Examiner, reversing the order of grinding or polishing does not provide a substantially identical or equivalent in terms of function, manner and result.

Moreover, the back side resin layer 4 is entirely removed in a manufacturing process of the semiconductor device according to the invention of amended claim 3, while the front side protective resin layer 3 remains on the semiconductor substrate of the semiconductor device as a final product. In this sense, it is important to make the thickness of the front side protective resin layer 3 uniform in any portion of the wafer W. Further, where projection electrodes T

are formed on the wafer W, the heights of the respective projection electrodes T depend on the thickness of the front side protective resin layer 3. Therefore, by making the thickness of the front side protective resin layer 3 uniform throughout the wafer W, the heights of the plurality of the projection electrodes T can be made uniform, resulting in more reliable semiconductor devices. These features of the invention are nowhere shown or suggested by the cited prior art.

In view of the above, amended claim 3, and claims 4 and 6 depending therefrom, are deemed clearly to be patentable over the cited prior art. The rejection of these claims accordingly should be withdrawn.

The Examiner rejected claim 10-25 under 35 USC 102(b) as being anticipated by *Sekine et al.* Claim 10 has been amended to include the limitations of claim 11 and explicitly to recite that the claimed method produces a chip-on-chip structure. Claims 11, 13-16 and 22-25 have been canceled. The rejection respectfully is traversed as to amended claim 10 and claims 12 and 17-21.

Claim 10 has been amended to recite that the solid device includes a second semiconductor chip so that the claimed semiconductor device includes first and second semiconductor chips defining a chip-on-chip structure. *Sekine et al.* clearly do not teach or even suggest a chip-on-chip structure. Therefore,

amended claim 10, and claim 12 depending therefrom are clearly patentable over *Sekine et al.*

Claim 17 has been amended to make explicit what is implicit in the recitation of the cutting out step, namely that the chip bonding step of bonding a plurality of semiconductor chips face-down onto a surface of a semiconductor substrate with active surfaces of the semiconductor chips opposed to the surface of the semiconductor substrate is performed in such a manner that the plurality of semiconductor chips and the substrate define chip-on-chip structures. *Sekine et al.* do not disclose manufacture of a device that includes chip-on-chip structure. Thus, for at least the reasons similar to those presented above that amended claim 10 is patentable over *Sekine et al.*, claim 17, and claims 18-21 depending therefrom are deemed to be clearly patentable.

Moreover, the dependent claims further distinguish the invention over the *Sekine et al.* The Examiner states that *Sekine et al.* disclose projection electrodes formed to be higher than the active surface of the semiconductor chip and lower than the inactive surface of the semiconductor chip. This assertion suggests a misunderstanding of the claim. That is, according to the invention, and contrary to *Sekine et al.*, each of the projection electrodes has a height such that the top end thereof is between the height of the active surface and a height of the inactive surface of the semiconductor chip. Claim 21 has been amended to make this limitation more clear.

Therefore, for all of the reasons advanced above, claims 10, 12 and 17-21 are clearly patentable over *Sekine et al.*, and the rejection of these claims thereover accordingly should be withdrawn.

The Examiner also rejected claims 10-16 under 35 USC 102(b) as being anticipated by *Egawa*. As previously noted, claims 11 and 13-16 have been canceled and claim 10 has been amended to include the limitations of claim 11, and to otherwise clarify that the solid device includes a second semiconductor chip so that the claimed semiconductor device includes first and second semiconductor chips defining a chip-on-chip structure. As in the case of *Sekine et al.*, *Egawa* clearly does not teach or even suggest a chip-on-chip structure. Claims 10 and 12 therefore are deemed clearly to be patentable over *Egawa* and the rejection accordingly should be withdrawn.

Therefore, based on the above, it is submitted that this application is in condition for allowance. Such a Notice, with allowed claims 3, 4, 6, 10, 12 and 17-21, earnestly is solicited.

Should the Examiner feel that a conference would help to expedite the prosecution of the application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such a conference. Should any additional fee be required, or if no payment is attached, please charge the same to our Deposit Account No. 18-0002 and advise us accordingly.

Respectfully submitted,

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Date

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